[10191/4188]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Werner HARTER et al. For: DEVICE AND METHOD FOR CREATING A SIGNATURE Filed: December 12, 2005 Serial No.: 10/539,495	Examiner: John P. Trimmings Art Unit: 2117

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Signature: /Aaron Grunberger/
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APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

SIR:

On June 19, 2008, Appellants submitted a Notice of Appeal from the last decision of the Examiner contained in the Final Office Action dated February 19, 2008 in the above-identified patent application.

In accordance with 37 C.F.R. § 41.37, this brief is submitted in support of the appeal of the final rejections of claims 11 to 20. For at least the reasons set forth below, the final rejections of claims 11 to 20 should be reversed.

1. REAL PARTY IN INTEREST

The real party in interest in the present appeal is Robert Bosch GmbH of Stuttgart, Federal Republic of Germany, which is the assignee of the entire right, title and interest in the present application.

2. RELATED APPEALS AND INTERFERENCES

There are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellants or the assignee, Robert Bosch GmbH, "which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal."

3. STATUS OF CLAIMS

Claims 1 to 10 have been canceled.

Claims 11, 12 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,199,184 (the "Sim" reference).

Claim 13 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the "Sim" reference.

Claims 14 to 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the "Sim" reference in view of Biswas, "Design of UED-AUED Codes from Berger's AUED Code," IEEE VLSI Design, pages 364-369 (the "Biswas" reference).

Appellants appeal from the final rejections of claims 11 to 20.

A copy of the appeal claims, *i.e.*, claims 11 to 20, is attached hereto in the Claims Appendix.

4. STATUS OF AMENDMENTS

In response to the Final Office Action dated February 19, 2008, Appellants submitted a "Response to Final Office Action" on April 28, 2008. However, the Response did not contain any amendments.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The presently claimed subject matter of independent claims 11 and 20 relate, respectively, to a device and method for forming a signature. Claims 11 and 20 include the features of, respectively, a shift register and the step of providing a shift register, where the shift register has a predefined number of bit position memory devices, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices after a predefined number of applied data words and cycles. *Specification*, page 2, lines 7 to 14; page 3, line 31 to page 4, line 5; Figure 3. Claims 11 and 20 further include the features of, respectively, a code generator and the step of providing a code

generator, where the code generator generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature. *Specification*, page 4, lines 7 to 30; Figure 4.

In summary, the presently claimed subject matter of claim 11 is to a device for forming a signature, comprising a shift register having a predefined number of bit position memory devices, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices after a predefined number of applied data words and cycles (*Specification*, page 2, lines 7 to 14; page 3, line 31 to page 4, line 5; Figure 3); and a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature. (*Specification*, page 4, lines 7 to 30; Figure 4; *See* claim 11).

Claim 12 depends from claim 11 and includes further features wherein the individual bit position memory devices are connected by antivalence points, and the individual bits of the data words at the antivalence points, as well as the at least one additional bit position of the code generator, are inserted to form the signature. (*See* claim 12).

Claim 13 depends from claim 11 and includes further features wherein the individual bit position memory devices are connected by equivalence points, and the individual bits of the data words, as well as the at least one additional bit position of the code generator, are inserted at the equivalence points to form the signature. (*See* claim 13).

Claim 14 depends from claim 11 and includes further features wherein the code generator implements an ECC code and inputs a number of bit positions corresponding to the ECC code being used into a corresponding number of additional bit position memory devices to form the signature. (*See* claim 14).

Claim 15 depends from claim 11 and includes further features wherein the code generator forms a parity bit and inputs it in an additional bit position memory device of the shift register. (*See* claim 15).

Claim 16 depends from claim 14 and includes further features wherein the code generator implements a Hamming code. (*See* claim 16).

Claim 17 depends from claim 14 and includes further features wherein the code generator implements a Berger code. (*See* claim 17).

Claim 18 depends from claim 14 and includes further features wherein the code generator implements a Bose-Lin code. (*See* claim 18).

Claim 19 depends from claim 14 and includes further features wherein the code generator implements a generic code generator table. (*See* claim 19).

The presently claimed subject matter of claim 20 is to a method for forming a signature, comprising: providing a shift register having a predefined number of bit position memory devices, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices after a predefined number of applied data words and cycles (*Specification*, page 2, lines 7 to 14; page 3, line 31 to page 4, line 5; Figure 3); and providing a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature. (*Specification*, page 4, lines 7 to 30; Figure 4; *See* claim 20).

The appealed claims include no means-plus-function language and no step-plus-function claims, so that 41.37(c)(1)(v) is satisfied as to its specific requirements for such claims, since none are present here.

6. GROUNDS OF REJECTIONS TO BE REVIEWED ON APPEAL

A. Whether claims 11, 12 and 20, which stand rejected under 35 U.S.C. § 102(b), are patentable over the "Sim" reference.

B. Whether claim 13, which stands rejected under 35 U.S.C. § 103(a), is patentable over the "Sim" reference.

C. Whether claims 14 to 19, which stand rejected under 35 U.S.C. § 103(a), are patentable over the "Sim" reference in view of the "Biswas" reference.

7. ARGUMENTS

A. Rejection of Claims 11, 12 and 20 Under 35 U.S.C. § 102(b)

Claims 11, 12 and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the "Sim" reference. It is respectfully submitted that the "Sim" reference does not anticipate any of claims 11, 12 and 20 for at least the following reasons.

It is "well settled that the burden of establishing a *prima facie* case of anticipation resides with the [United States] Patent and Trademark Office." *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1788 to 1789 (Bd. Pat. App. & Inter. 1986). To anticipate a claim, each

and every element as set forth in the claim must be found in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of Calif.*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). That is, the prior art must describe the elements arranged as required by the claims. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

i. Claims 11 and 20

Each of claims 11 and 20 relates to a code generator which generates at least one additional bit position *in at least one additional bit position memory device of the shift register* from each applied data word in the signature. The "Sim" reference does not disclose, or even suggest, a code generator as provided for in claims 11 and 20.

As an initial matter, the Examiner has not addressed this feature, but has instead determined that these words are a mere technicality. *See* Advisory Action. However, all words of a claim must be considered. No words of a claim can be overlooked as a "mere technicality." Since the Examiner has not shown where or how the "Sim" reference discloses this feature and since this disclosure is not apparent in the "Sim" reference, for at least this reason, the Examiner has not established a *prima facie* case of anticipation.

Further, it is clear that the "Sim" reference does not disclose, or even suggest, this feature. The Final Office Action refers to the second multiple input signature register (MISR) 42-2 of Figure 4 of the "Sim" reference as disclosing the code generator of claims 11 and 20. However, MISR 42-2 does not generate any bit positions in any additional bit position memory devices of the shift register, as provided for in the context of claims 11 and 20. In this regard, the Final Office Action identifies MISR 42-1 as disclosing the shift register of claims 11 and 20. However, it is evident from Figure 4 and corresponding text of the "Sim" reference that MISR 42-2 and MISR 42-1 are separate and distinct shift registers coupled in series and that the 6 bit positions of MISR 42-2 are not in at least one additional bit position memory device of the separate and distinct shift register MISR 42-1 referred to by the Examiner as assertedly disclosing the shift register of claims 11 and 20.

In this regard, page 4, lines 7 to 14 of the specification and Figure 4 of the present application describes an example embodiment of the features of claims 11 and 20 where an MISR is extended by an i bit code generator 407 and at least one additional flip-flop. In contrast, MISR 42-2 of the "Sim" reference does not add any bit positions to any bit position memory devices of MISR 42-1.

Further, as described in column 5, lines 19 to 21 of the "Sim" reference, the output of MISR 42-1 is fed into a corresponding input of MISR 42-2. MISR 42-2 receives the output of MISR 42-1, offset by one bit. This arrangement requires a large number of flip-flops and XOR gates for integrating the two MISRs. For each bit of an MISR, flip-flops will be required for connection to preceding and following MISRs, as well as XOR gates for the feedback polynomials depicted in Figures 4 and 5 of the "Sim" reference. In this regard, where MISRs are serially connected as in the "Sim" reference, all MISRs have the same feedback polynomials, but differ only in regard to their input signals. While the primary data is made available to the first of the serially connected MISRs, the subsequent MISRs respectively process the outputs of the preceding MISRs, typically offset by one bit. However, for n bit MISRs, the expenditure is at least 2n, 3n, or even 4n flip-flops plus the respectively necessary EXORs for integrating the inputs – 2n, 3n, or 4n EXORs, and the EXORs for the feedback in accordance with the respectively selected polynomial.

In contrast, the present application provides for a code generator that, for example, receives the applied data directly and generates at least one additional bit position in at least one additional bit position memory device of the shift register. The arrangement of the present invention permits the operation of the code generator, for example, as a parity generator, minimizing the number of flip-flops and XOR gates required to integrate the code generator with the remainder of the arrangement.

Further, the "Sim" reference does not disclose, or even suggest, a code generator that generates the at least one additional bit position from *each applied data word* in the signature. MISR 42-2, considered by the Examiner to disclose the code generator of claim 11, does not generate any bit positions from each applied data word. MISR 42-2 is not provided with the applied data words; the inputs to MISR 42-2, as described above, are linked to the outputs of MISR 42-1. MISR 42-2, then, cannot generate additional bit positions *from the applied data words*.

As such, MISR 42-2 of the "Sim" reference does not disclose, or even suggest, the code generator of claims 11 and 20. The "Sim" reference does not disclose, or even suggest, any another features that anticipate the code generator featured in claims 11 and 20. Therefore, the "Sim" reference does not anticipate independent claims 11 and 20.

In view of all of the foregoing, reversal of this rejection of claims 11 and 20 is respectfully requested.

ii. Claim 12

With respect to claim 12, as an initial matter, claim 12 depends from claim 11 and therefore incorporates all of the features of claim 11. As explained above, the "Sim" reference does not anticipate claim 11, from which claim 12 depends. Therefore, the "Sim" reference does not anticipate claim 12 for at least the same reasons as claim 11.

Further, claim 12 provides that the individual bits of the data words at the antivalence points, as well as the at least one additional bit position of the code generator, are inserted to form the signature. The "Sim" reference does not disclose, or even suggest, this feature. The "Sim" reference describes the application of input data to MISR 42-1, which yields a signature. To test the signature, MISR 42-2 is used to shift the output of MISR 42-1, creating a second signature. In contrast, in the present application, the output of the shift register is inserted, along with the additional bit position of the code generator, to form the signature. Because the "Sim" reference does not disclose, or even suggest, this insertion of both the individual bits of data words and the at least one additional bit position of the code generator, the "Sim" reference does not anticipate claim 12.

In view of all of the foregoing, reversal of this rejection of claim 12 is respectfully requested.

B. Rejection of Claim 13 Under 35 U.S.C. § 103(a)

Claim 13 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the "Sim" reference. It is respectfully submitted that the "Sim" reference does not render unpatentable claim 13 for at least the following reasons.

Claim 13 depends from claim 11 and therefore incorporates all of the features of claim 11. As more fully set forth above with respect to claim 11, the "Sim" reference does not disclose, or even suggest, all of the features of claim 11. As such, the "Sim" reference does render unpatentable independent claim 11, or dependent claim 13.

Reversal of this rejection of claim 13 is therefore respectfully requested.

C. Rejection of Claims 14 to 19 Under 35 U.S.C. § 103(a)

Claims 14 to 19 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the "Sim" reference in view of the "Biswas" reference. It is respectfully submitted that the combination of the "Sim" and "Biswas" references does not render unpatentable claims 14 to 19 for at least the following reasons.

i. Claims 14 and 16 to 19

Claims 14 and 16 to 19 ultimately depend from claim 11 and are therefore allowable for at least the same reasons set forth above in support of the patentability of claim 11, since the "Bisaws" reference does not cure the critical deficiencies noted above with respect to the "Sim" reference.

Reversal of this rejection of claims 14 and 16 to 19 is therefore respectfully requested.

ii. Claims 15

With respect to claim 15, as an initial matter, claim 15 depends from claim 11 and is therefore allowable for at least the same reasons set forth above in support of the patentability of claim 11, since the "Bisaws" reference does not cure the critical deficiencies noted above with respect to the "Sim" reference.

Further, claim 15 provides that the code generator forms a parity bit and inputs it in an additional bit position memory device of the shift register. The "Sim" reference is directed to the use of shift registers to check the accuracy of a signature. The "Biswas" reference, however, is not directed to the use of shift registers and provides no suggestion for modification of a shift register arrangement. As such, neither of the cited references suggest modification of a shift register arrangement, where a shift register is modified. Instead, the references, even when combined, at most suggest modification of a shift register arrangement by inclusion of a multiplicity of shift registers. The combined references would not suggest to one skilled in the art modification of a shift register arrangement to yield the arrangement of claim 15, where a code generator forms a parity bit and inputs the bit into an additional bit position memory device of a shift register.

In view of all of the foregoing, reversal of this rejection of claim 15 is respectfully requested.

8. CLAIMS APPENDIX

A "Claims Appendix" is attached hereto and appears on the 2 (two) pages labeled "Claims Appendix 1" and "Claims Appendix 2."

9. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellants in the appeal. An "Evidence Appendix" is nevertheless attached hereto.

10. RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2, above, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellants or the assignee, Robert Bosch GmbH, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there are no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted. A "Related Proceedings Appendix" is nevertheless attached hereto.

11. CONCLUSION

For at least the reasons indicated above, Appellants respectfully submit that the art of record does not disclose or suggest the subject matter as recited in the claims of the above-identified application. Accordingly, it is respectfully submitted that the subject matter recited in the claims of the present application is new, non-obvious and useful.

In view of all of the foregoing, reversal of all of the rejections set forth in the Final Office Action is therefore respectfully requested.

Respectfully submitted,

Dated: August 7, 2008

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CLAIMS APPENDIX

11. A device for forming a signature, comprising:

a shift register having a predefined number of bit position memory devices, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices after a predefined number of applied data words and cycles; and

a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature.

12. The device according to claim 11, wherein the individual bit position memory devices are connected by antivalence points, and the individual bits of the data words at the antivalence points, as well as the at least one additional bit position of the code generator, are inserted to form the signature.

13. The device according to claim 11, wherein the individual bit position memory devices are connected by equivalence points, and the individual bits of the data words, as well as the at least one additional bit position of the code generator, are inserted at the equivalence points to form the signature.

14. The device according to claim 11, wherein the code generator implements an ECC code and inputs a number of bit positions corresponding to the ECC code being used into a corresponding number of additional bit position memory devices to form the signature.

15. The device according to claim 11, wherein the code generator forms a parity bit and inputs it in an additional bit position memory device of the shift register.

16. The device according to claim 14, wherein the code generator implements a Hamming code.

17. The device according to claim 14, wherein the code generator implements a Berger code.

18. The device according to claim 14, wherein the code generator implements a Bose-Lin code.

19. The device according to claim 14, wherein the code generator implements a generic code generator table.

20. A method for forming a signature, comprising:

providing a shift register having a predefined number of bit position memory devices, to which input data to be tested is applied bit-by-bit and in parallel as successive data words and which serially shift the input data forward in a predefined cycle, a signature being formed in the bit position memory devices after a predefined number of applied data words and cycles; and

providing a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature.

EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellants in the appeal.

RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2 of this Appeal Brief, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellants or the assignee, Robert Bosch GmbH, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted.